REMARKS

Upon entry of this amendment, claims 1-7, 14, 17, 31, 43, and 54-64 will be pending. Claim 28 has been cancelled. Claims 14, 17, 31, and 54 have been amended. Support for the amendment to claim 14 with regard to a "semiconductor integrated circuit device substrate" may be found in the specification at paragraph 0001. Support for new claims 60-64 can be found, for example, in original claims 15-19.

No additional claim fees are believed to be due because there are currently 22 claims including five independent claims. The original filing fees covered 53 total claims including six independent claims.

§ 112 Rejection of Claim 54

Reconsideration is requested of the rejection of claim 54 under §112. Claim 54 has been amended to address the rejection. Applicants therefore request withdrawal of the §112 rejection.

§ 103(a) Rejection of Claims 14 and 54-59

Reconsideration is requested of the rejection of claims 14 and 54-59 as being obvious over Kardos et al. (U.S. 3,956,078) in view of Dubin et al. (U.S. 5,972,192).

Claim 14 is directed to a method for electroplating a copper deposit onto a semiconductor integrated circuit device substrate having electrical interconnect features including submicron-sized features such that the surface has submicron-sized reliefs therein, the method comprising

> immersing the ***semiconductor integrated circuit device substrate*** into an electroplating bath...; and
>
> electroplating the copper deposit from said bath onto the ***semiconductor integrated circuit device substrate*** to fill the submicron sized reliefs...

Kardos et al.'s relevant substrates are printed circuit boards (PCBs) (Col. 1, line 60), and do not include "semiconductor integrated circuit device substrates." To underscore the distinction between claim 14 and the Kardos et al. method, claim 14 has been amended to specify "semiconductor integrated circuit device substrate." The Kardos et al. method does not pertain to copper filling of interconnects in semiconductor integrated circuit device substrates.

Per MPEP 2141.01(a), a reference may be relied upon as a basis for a section 103 rejection only if it is "analogous prior art," which includes references either (1) in the field of the applicants' endeavor or (2) those that are reasonably pertinent to the particular problem with which the applicants were concerned. In this particular instance, the Kardos et al. patent was based on an application filed more than 30 years ago and related to copper plating in the manufacture of PCBs. Printed circuit boards of 30 years ago and even PCBs of today are not in the same field as applicants' copper filled vias and trenches of integrated circuits. Printed circuit boards are relatively large substrates, and are boards which electronic components are plugged into or otherwise mounted onto and then electrically connected to each other by wiring formed by printing copper patterns. Printed circuit boards are typically a resinous material several inches on a side. In the process disclosed by Kardos et al., Cu was plated onto solid brass panels scratched with 4/0 emory polishing paper over a horizontal band of about ***10 mm. width***. (Col. 12, lines 32-46). Copper is deposited onto the entire surface as by Kardos et al.'s process and wiring patterns are created either by masking or etching.

In contrast to PCBs, an integrated circuit is a combination of interconnected individual circuit elements inseparably associated with each other within a continuous substrate. An IC is a semiconductor material such as SiO_2 typically only several

millimeters on a side or smaller. Copper is deposited with the goal of completely filling vias and trenches with openings of submicron sized, e.g., ***0.5 microns and lower*** which serve as micro, solid-state interconnects between microelements. (Applicants' specification, at ¶0003).

PCBs are macro-scale carriers of electronic signals between electronic components; whereas ICs are miniaturized electronic components. By analogy, PCBs are an interstate highway system; whereas ICs are automobiles on that system.

Inasmuch as plating of PCBs and filling vias and trenches in ICs are distinct fields of endeavor, therefore, Kardos et al. cannot fairly be relied on under the first analogous art test of MPEP 2141.01(a).

Having failed the first condition under MPEP 2141.01(a), Kardos et al. can only be applied as a basis for rejection under Section 103 if it is "reasonably pertinent to the particular problem with which the inventors were concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). In this instance, the problem with which the inventors were concerned was filling sub-micron sized vias and trenches with copper such that the Cu deposit undergoes a reduced rate of recrystallization and grain growth. As stated in the specification, the main problem with filling these via and trench features is that they are extremely small, as small as 0.5 micron or less in width; and after deposition, the deposited Cu has a tendency to recrystallize and form large grains, thus yielding stress-induced defects. (Applicants' specification, at ¶0016). Further problems with stress-induced defects include detachment of the deposit from the via and trench walls, and the formation of spontaneous internal voids. These geometries and the problem of filling copper in a void-free manner, both during and after deposition, are wholly unique to the recent several years, as copper has replaced aluminum as the interconnect metal on

semiconductor IC substrates and as the miniaturization of devices has forced features into the submicron size range. These conditions were not imaginable 30 years ago when Kardos et al. was issued. But more importantly, these conditions are unique to today's IC manufacturers, and are not encountered in PCB processing - neither today nor 30 years ago.

Most significantly, in copper filling of vias and trenches it is necessary to "superfill," i.e., fill copper into the feature faster than one deposits copper onto the surrounding substrate. What is required, therefore, is non-conformal deposition; i.e., deposition which does not conform to the overall shape of the substrate. In contrast, non-conformal deposition is not an overriding concern in depositing Cu on PCBs. Rather, generally conformal deposition is desired in Cu plating PCBs. There are a number of other distinctions, such as the distinctions between the types of substrates; but this distinction between the overall goals of the processes -- conformal deposition versus non-conformal filling -- is so fundamental that it establishes that Kardos et al. is not "reasonably pertinent to the particular problem [i.e., non-conformal filling] with which the inventor was concerned."

As plating copper on PCBs addresses a wholly different set of concerns, one skilled in the art of filling vias and trenches on semiconductor IC substrates would not have reasonably looked to Kardos et al. to provide guidance. Therefore, Kardos et al. cannot fairly be deemed to be analogous art to claim 14 because the problems encountered by them are not reasonably pertinent to those encountered by applicants.

Even if the Kardos et al. reference were either in the same field or reasonably pertinent to the same problem as claim 14, Kardos et al. and Dubin et al. do not render the subject matter of claim 14 obvious because there is no suggestion or motivation

to make the proposed modification. In the context of establishing a prima facie case of obviousness under §103(a),

> First, there must be ***some suggestion or motivation***, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to ***modify the reference*** or ***to combine reference teachings***. MPEP 2143, first paragraph.

It is asserted in the Office Action at page 5 that Dubin et al. teaches that copper plating compositions useful to plate circuit board substrates with small diameter, high aspect ratio microvias and other apertures will be useful to plate integrated circuit devices, such as semiconductor devices, relying on Dubin et al.'s text in columns 7 and 8. Applicants respectfully request reconsideration of the Office's reliance on this text in Dubin et al. for this proposition. In particular, this passage only states that the "electroplating compositions employed in the present invention for electroplating Cu or a Cu alloy are conventional...." (Col. 7, line 58). It does not state whether they are "conventional" for semiconductor integrated circuit devices, or for PCBs. In fact, the entire Dubin et al. document is wholly devoid of any reference to Cu plating of PCBs. Accordingly, one can only reasonably assume that "conventional" refers to "semiconductor integrated circuit plating" and not to PCB plating.

Stated another way, Kardos et al. only refer to PCB plating. Dubin et al. only refer to semiconductor integrated circuit plating. Dubin et al. make no suggestion, express or implied, that PCB plating chemistries can be applied to semiconductor integrated circuit plating. There is no basis in either reference to conclude there is any reasonable expectation of success in applying Kardos et al.'s PCB chemistries to the disparate application of superfilling sub-micron sized features in semiconductor integrated circuit substrates. There is simply

no basis in either reference, without relying on conjecture, "possibilities or probabilities", or impermissible "obvious-to-try" type logic, to make the technical leap of applying Kardos et al.'s chemistries to applicants' substrates.

It is further significant that the gist of Dubin et al.'s invention is to include components in the copper plating solution to ***increase*** grain size. (Col. 6, lines 1-14). The resulting Cu deposits in Dubin et al. exhibited "significantly ***increased*** grain size." (Col. 6, lines 35-58). Accordingly, taking the references as a whole, if one of ordinary skill in the art had expected that any of the components in Kardos et al.'s chemistries (such as the polyvinylpyridine noted in the Office action) would have inherently "reduced a rate of recrystallization and grain growth in the copper deposit" as expressly required in applicants' claim 14, that person would have been motivated by Dubin et al. to AVOID such a component.

In view of i) the non-analogous nature of Kardos et al. with respect to applicants' invention, ii) the absence of any motivation in either reference to make the proposed modification and apply Kardos et al.'s chemistries to semiconductor IC substrates, iii) the lack of any technical basis to expect success, and iv) the teaching of Dubin et al. away from the claimed invention, therefore, applicants respectfully request withdrawal of the rejection of claim 14.

Claims 54-59 depend from claim 14 and are patentable for the same reasons as claim 14 and by virtue of the additional requirements therein.

§ 103(a) Rejection of Claim 28

Claim 28 has been canceled.

Objections to Claims 17 and 31

Claims 17 and 31 have been amended to be independent and include all the limitations of their respective base claims.

New Claims 60-64

Claims 60-64 correspond to original claims 15, 16, 18, and 19, and are directed to species which were not elected for examination. Claim 14 is generic to and readable upon these claims. As noted on page 4 of the December 9, 2003 Office action, and consistent with 37 CFR 141, upon allowance of a generic claim such as claim 14, applicants are entitled to consideration of claims such as 60-64 directed to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim.

Supplemental Information Disclosure Statement

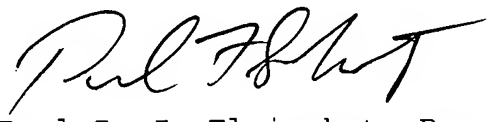
* Applicants enclose a Supplemental Information Disclosure Statement.

CONCLUSION

In view of the above, allowance of claims 1-7, 14, 17, 31, 43, and 54-64 is respectfully requested.

A check is enclosed for payment of the one-month extension of time fee. The Commissioner is hereby authorized to charge any underpayment and credit any overpayment of government fees to Deposit Account No. 19-1345.

Respectfully submitted,



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